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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,659	07/27/2004	Chung-Chieh Chang	10318-US-PA	4658
	7590 01/31/200' NINTELLECTIAL PI	EXAMINER		
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE 7 FLOOR-1, NO. 100			KITOV, ZEEV V	
ROOSEVELT ROAD, SECTION 2 TAIPEI, 100		ART UNIT	PAPER NUMBER	
TAIWAN			2836	
			MAN DATE	DELIVERY MODE
			MAIL DATE	
			01/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

9)

Supplemental Notice of Allowability

Application No.	Applicant(s)		
10/710,659	CHANG ET AL.		
Examiner	Art Unit		
Zeev Kitov	2836		

Notice of Allowability	Examiner	Art Unit				
	Zeev Kitov	2836				
The MAILING DATE of this communication appe All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this app or other appropriate communication GHTS. This application is subject to	olication. If not includ will be mailed in due	ed course. THIS			
1. This communication is responsive to <u>06/22/05</u> .			•			
2. The allowed claim(s) is/are <u>1 - 5, 7 - 9, 11, 12, 14 - 18</u> .						
 3. Acknowledgment is made of a claim for foreign priority unall All b) Some* c) None of the: Certified copies of the priority documents have Certified copies of the priority documents have Copies of the certified copies of the priority documents have Copies of the certified copies of the priority documents have Tertified copies of the certified copies of the priority documents have Certified copies not received:	been received. been received in Application No cuments have been received in this in of this communication to file a reply of ENT of this application. itted. Note the attached EXAMINER' its reason(s) why the oath or declarant be submitted.	national stage applicational stage applicational stage application of the recomplying with the recomplishing with	quirements			
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached1) ☐ hereto or 2) ☐ to Paper No./Mail Date						
(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date						
Identifying indicia such as the application number (see 37 CFR 1. each sheet. Replacement sheet(s) should be labeled as such in the			back) of			
6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.						
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Attachment(s) 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. Notice of Informal Page 1. Interview Summary Paper No./Mail Dat 7. Examiner's Amendn 8. Examiner's Stateme 9. Other	(PTO-413), e nent/Comment	wance			

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REASONS FOR ALLOWANCE

Examiner acknowledges a submission of the amendment and arguments filed on June 22, 2005. Claim 6 is deleted; Claim 1 is amended. Amendment and arguments have overcome rejections under 102 (b) and 103(a).

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Attorney, Mrs. Belinda Lee on January 9, 2007.

- 1. Please cancel Fig. 5 Drawings.
- 2. Please cancel Amendment to Specification dated 06/27/2006 and New Sheet of Drawings (Fig. 6) dated 06/27/2006.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

An amended independent Claim 5 discloses a control circuit for a frequency converter, which inter alia, includes: the first parallel circuit including a switch circuit, being turned on or off by a starter circuit, and a timer switch connected in parallel to the switch circuit

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to form the first parallel circuit; and a second parallel circuit, for turning on or off the frequency converter, wherein the fist parallel circuit and the second parallel circuit are connected in series, the second parallel circuit including a starter relay, wherein when a voltage level of the power supply is below a first predetermined voltage level, the starter relay is turned off, and when the voltage level of the power is above a second predetermined voltage level, the starter relay is turned on; and a timer relay, wherein when the voltage level of the power supply is below the first voltage level, the timer relay remains being turned on for a predetermined time period and to keep the first parallel circuit receiving the power source, which keeps the frequency converter on, wherein during the predetermined time period, if the voltage level of the power supply is increased to the first predetermined level, the frequency converter remains turned on keeping the equipment being operated normally, wherein after the predetermined time period, if the voltage level of the power supply is still below the second voltage level, the timer relay is turned off and the frequency converter is also turned off.

The closest reference for the claim is Applicant Admitted Prior Art, which discloses some elements of the claim, such as starter circuit, switch circuit, starter relay, frequency converter and load equipment. However, it does not disclose the timer relay with its contacts in parallel to the switch circuit. Another reference Matsko discloses the circuit wherein when the voltage level of the power supply to the control circuit is raised to above a second predetermined voltage level defined by the zener diode (element ZD5 in Fig. 1) voltage and the voltage divider R10, R13 and R6 (the resistor

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R7 is shorted by saturated output of comparator CO3) (see col. 6, lines 18 – 47), the starter relay (element UVRC in Fig. 1) is turned on.

It further discloses a timer relay (elements R1 – R3, C1 – C3, CO1 – CO3 in Fig. 1), wherein when the voltage level of the power supply to the control circuit is below the first predetermined voltage level defined by the zener diode (element ZD5 in Fig. 1) voltage and the voltage divider R10, R13, R6 and R7 (the R7 is not is shorted by the floating output of comparator CO3) (see col. 6, lines 18 – 47), the starter relay (element UVRC in Fig. 1) remains on for a predetermined time period defined by the delay circuit (elements C1 – C3, R1 – R3 in Fig. 1). The timer relay determines whether or not to turn on/off the timer switch (element UVRC in Fig. 1).

However, it does not disclose the timer switch connected in parallel to the switch circuit.

Allowability resides, at least in part, in the above-described limitations, which has not been disclosed in the Prior Art in a search.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose telephone number is (571) 272-2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on

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(571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K. 1/23/2007

STEPHEN W. JACKSON PRIMARY EXAMINER